SEP 0 7 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Bruno GHYSELEN et al.
Confirmation No. 7267

Application No: 10/686,082
Group Art Unit: 2812

Filing Date: October 14, 2003
Examiner: L. Schillinger

Atty. Docket No.: 4717-11400

For: PREVENTIVE TREATMENT METHOD FOR A MULTILAYER SEMICONDUCTOR STRUCTURE

APPEAL BRIEF FEE TRANSMITTAL

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Respectfully submitted,

Date: 9/7/2006

Jasbir Singh

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BRIEF FOR APPELLANTS

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Sir:

Applicants appeal to the Board of Patent Appeals and Interferences (the "Board") from the decision of the Examiner mailed January 10, 2006 rejecting claims 1, 3-7 and 9-19 that are reproduced in Appendix A of this brief.

1. REAL PARTY IN INTEREST

The real party in interest is S.O.I. TEC Silicon on Insulator Technologies S.A. (hereafter "Soitec"), having a business address of Parc Technologique des Fontaines, Chemin des Franques, 38190 Bernin, FRANCE, the assignee of the entire right, title, and interest in the invention described and claimed in the above-identified patent application. Bruno Ghyselen and Olivier Rayssac assigned the invention to Soitec. The assignment was recorded on October 14, 2003 on Reel 014670 at Frames 0090-93.

2. RELATED APPEALS AND INTERFERENCES

Appellants and its legal representatives are not aware of any appeal or interference that directly affects, will be directly affected by, or will have a bearing on the Board's decision in this appeal.

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3. STATUS OF CLAIMS

Claims 1-20 were submitted upon filing of application 10/686,082. In a response to a restriction requirement mailed March 23, 2005, applicants elected method claims 1-19 on March 28, 2005 with traversal. In an Office Action dated June 27, 2005, claims 1-20 were rejected as not enabled; claims 1-20 were rejected as being anticipated by U.S. Patent No. 6,902,987 to Tong et al. ("Tong"). A response was filed on September 13, 2005, wherein claims 2 and 8 were cancelled and claims 1, 3-5, 12, 15-17 and 19-20 were amended.

In a Final Office Action mailed January 10, 2006, the Examiner withdrew claim 20 and claims 1, 3-7 and 9-19 were rejected as anticipated by Tong. A Response to the Final Office Action was filed January 30, 2006. None of the pending claims were amended in that response.

An Advisory Action mailed March 22, 2006, indicated that the Response to the Final Office Action did not place the application in condition for allowance because a side-by-side study was not submitted. A Pre-Appeal Brief Request for Review was filed on March 31, 2006. A Notice of Panel Decision from Pre-Appeal Brief Review was mailed on May 5, 2006, indicating that the application remains under appeal because there is at least one actual issue for appeal.

Claims 1, 3-7 and 9-19 have been twice rejected in their present form.

Claims 1, 3-7 and 9-19 are presented in Appendix A.

4. STATUS OF AMENDMENTS

Claim 2 and 8 have been cancelled, and claims 1, 3-5, 12, 15-17 and 19 have been amended.

In a response to a restriction requirement filed March 28, 2005, method claims 1-19 were elected with traversal.

In an amendment filed on September 13, 2005, claims 2 and 8 were cancelled and claims 1, 3-5, 12, 15-17 and 19-20 were amended.

A Response to the Final Office Action was filed January 6, 2006, making no amendments.

A Pre-Appeal Brief Request for Review was filed on March 31, 2006.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention generally relates to a preventive treatment method for a multilayer semiconductor structure having a support substrate, at least one intermediate layer and a surface layer in which the surface layer is to be subjected to a subsequent chemical treatment. The method includes forming a protective layer between the intermediate layer and the surface layer. The protective layer is made from a material chosen to be sufficiently resistant to the chemical treatment to protect the intermediate layer from chemical attack

Independent claim 1 defines a method for preparing a multilayer semiconductor structure that includes a support substrate, at least one intermediate layer of insulator material and a surface layer of semiconductor material in which the surface layer is to be subjected to a subsequent chemical treatment. A protective layer is formed between the intermediate insulating layer and the surface layer of the structure.. This protective layer protects the insulating layer from the subsequent chemical treatments to which the structure is exposed after the structure is formed. The structure is formed by bonding a donor substrate to the support substrate; and then transferring at least a surface layer from the donor substrate to the support substrate by a layer transfer technique to form a multilayer structure. Then, the surface layer of the multilayer structure can be chemically treated, e.g., with hydrofluoric acid, without attacking the insulating layer due to the presence of the protecting layer.

The present invention provides unexpected advantages conferred by improvement in the quality of useful layers in a multilayer substrate by reducing the defect density by making it more difficult for chemical species to access the buried layer and therefore almost entirely prevents etching of the buried layer "from the inside" of the structure. Other improvements provide for use of chemical species that are more aggressive and thus do not detrimentally affect the buried layer during the chemical treatment. A further improvement is that the present method results in a significantly reduced edge delamination effect. When a protective coating is provided in the structure 10, edge delamination of the removable substrate is non-existent or is minimal. Further, the edge delamination of the surface layer is approximately zero, because the annular recess facilitates initiation of separation at the weakened zone when mechanical separation forces are applied. These unexpected benefits support the patentbility of the present claims.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

In the final office action, claims 1, 3-7 and 9-19 were again rejected as being anticipated by US patent 6,902,987 to Tong et al. ("Tong"). Applicants submit that this rejection is in error and are seeking further review and reversal of the rejection by this appeal.

7. ARGUMENT

The Examiner's rejections of the pending claims are in error because the method of the invention are neither taught nor suggested in the disclosure in Tong, and the present claims are therefore not anticipated or rendered obvious by Tong. For the reasons below, Appellants respectfully request that the Examiner's anticipation rejection be reversed, and that claims 1, 3-7, and 9-19 be allowed.

It is well settled that anticipation, under 35 U.S.C. 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in single prior art reference. ***Kalman v. Kimberly-Clark Corp.***, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); ***Richardson v. Suzuki Motor Co.***, 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied*, 110 S.Ct. 154 (1989). The term "anticipation," in the sense of 35 U.S.C. 102, has acquired the accepted definition meaning "the disclosure in the prior art of a thing substantially identical with the claimed invention." ***In re Schaumann***, 572 F.2d 312,197 USPQ 5 (CCPA 1978). The initial burden of establishing a basis for denying patentability to a claimed invention rests upon the examiner. ***In re Fine***, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); ***In re Thorpe***, 777 F.2d 695, 227 USPQ 964 (Fed. Cir. 1985); ***In re Piasecki***, 745 F.2d 1468, 223 USPQ 785 (Fed. Cir. 1984). To satisfy this burden, therefore, each and every element of the claimed invention must be shown by the Examiner to be disclosed in Tong. Appellant respectfully asserts that the record fails to meet this-requirement.

The recited method requires amongst other things "forming a protective layer between the intermediate layer and the surface layer" and "forming a structure by bonding a donor substrate to the support substrate; and then transferring at least the surface layer from the donor substrate to the support substrate by a layer transfer technique to form the multilayer semiconductor structure." Thus, the surface layer of the multilayer structure is transferred to the structure from a donor substrate, while the protective layer, which is made from a material chosen to be sufficiently resistant to the chemical treatment, protects the intermediate layer from chemical attack during the subsequent chemical treatment of the surface layer. Tong fails to disclose or suggest among other things forming a protective layer according to the claimed invention.

In the rejection of record, various portions of the specification and drawing figures are pointed out as supportive description for several pages of narrative in the Office Actions. Appellant has carefully considered the Tong patent with particular scrutiny on those portions identified by the Office Actions. Appellant can find no explicit teaching in Tong of at least one element required by claim 1, nor any basis for inferring that such element is inherent in the reference. It is submitted that the Office Actions do not establish that Tong, although large in its disclosure, satisfies all of the above-described requirements of claim 1.

Tong discloses a method for bonding surfaces at low temperature by etching first and second bonding surfaces before bonding them together at room temperature. The etching is used to roughen the surfaces so that different materials can be bonded together. The surface roughness may be in a range of 0.1 to 3 nm. The preparation of the surfaces (see Figs. 1 and 2) consists of (1) forming bonding layers (col. 5 lines 6-15); (2) conducting an etching step to improve planarity and roughness (col. 5 lines 31-40); (3) polishing layer surfaces (col. 5 lines 16-30), further etching to activate the bonding layer surfaces (by VSE: Very Slight Etch, Plasma, RIE ...) (col. 5 line 41 to col. 6 line19), conducting a post VSE process by immersing the wafers in a chemical solution to terminate the surfaces (col. 6 lines 30-57), and then, bonding the surfaces together at room temperature (col. 6 line 59 to col. 8 line 22).

Tong thus discloses a method for bonding two wafer surfaces at room temperature wherein different chemical treatments are used during the preparation of the wafer surfaces and prior to bonding. Fig. 3C is referenced in office action (point 1), but this does not disclose the present invention, because Fig. 3 shows a structure having a bonding layer 32 having a free face, and a layer 31. If one considers the structure disclosed by Tong in Fig. 3C, in combination with the disclosure at col. 5 lines 35-40, a silicon nitride layer can be inserted inside the bonding layer 32. This means that a silicon nitride layer will divide the bonding layer 32 in two parts: 1) the upper bonding layer 32 which has a free face and could be considered to be the equivalent of the surface layer of the present invention. and 2) the lower portion of the bonding layer 32 which could be assimilated to the intermediate layer 2 of the present invention.

At best, Tong discloses that an additional layer of a nitride can be used to protect the remaining structure when a surface oxide later is to be removed. According to this interpretation, Tong "protects" the rear or non-exposed surface of the layer with the silicon nitride layer which is resistant to the etching solutions used to remove the surface oxide layer. To use Tong as a teaching of the presently claimed invention, a skilled artisan would find that Tong's silicon nitride layer is not protecting the oxide layer, since the oxide layer is provided on the surface and is intended to be removed. This is the exact opposite to what is claimed in the present invention. The protective layer is used to protect the internal oxide layer from etching that can occur when etching solutions passes through defects in the surface layer. Furthermore, Tong's bonding layer is not made of a protective material as he clearly discloses that the layer is etched to provide enhanced bonding properties. In contrast, the present claims recite the protection of an intermediate insulating layer by a layer of a protecting material that is provided between the thin layer and the intermediate insulating layer, and the surface layer is not removed. Neither the present structure nor the function of the different layers is disclosed by any possible reading of Tong.

Furthermore, the composition of the surface and intermediate layers disclosed by Tong are different than in the invention. Tong's surface layer and intermediate layer have the same composition, (see Fig. 3C) while in the present invention, the surface layer material is a semiconductor material while the intermediate buried layer is an insulating layer. Consequently, as the surface layer 32 of Tong has the same composition as the intermediate layer, it certainly will be etched by a chemical solution that etches the surface layer. In fact, Tong's invention requires that the material be etched to improve bonding so he certainly would not use a protective material to prevent etching, as that would negate what he is teaching as a benefit by providing such a surface layer. Thus, Tong's surface layer is not made from a material chosen to be sufficiently resistant to the chemical treatment to protect the intermediate layer from chemical attack, as recited in claim 1. Thus, Tong does not disclose or inherently result in the presently claimed invention.

In col. 5 lines 31-40, Tong discloses that the etching and polishing are realized directly on the bonding layer 32 to improve the roughness of that surface. The use of a silicon nitride layer as a protective layer is suggested to limit the attack of the SiO_2 bonding layer 32 by the HF that is applied during the smoothing step. In contrast, in the present invention, the semiconductor surface layer is not eliminated with the chemical treatment used to attack the intermediate insulating layer [0026], [0033], since this chemical attack is performed after manufacturing of the full structure (surface layer, intermediate layer, protection layer) and the protective layer prevents further attack beyond the surface layer.

Therefore, the silicon nitride layer disclosed in the Tong is used to prepare the bonding layer before bonding the wafers to form the final structure, rather than to protect subjacent layers in the final structure as in the present invention. In the present invention, this protective layer prevents attack of the buried insulating layer by the chemical treatments occurring after the fabrication of the final substrate, and of course after the bonding step (Figs. 5 to 9 and [0010] of the published application). And nowhere in Tong is it suggested or disclosed that a chemical treatment realized after the bonding step, on the surface layer of the bonded structure, could lead to defects in the intermediate layer that could be prevented by the provision of a protective layer.

The comments on the last page of the final office action seem to be directed to different claims than the ones that are currently of record. Applicants are at a loss to explain why the present rejection has been made, and requests for interviews with the Examiner and the appeal conference members to better understand the basis for the rejection was denied. Clearly, each of the claim recitations that are relied upon for patentability are certainly present in independent claim 1, and all other claims depend upon claim 1. Thus, the present rejection should be reversed so that the present claims can be allowed, With the reversal of the current rejection, claim 20 should be rejoined and also allowed with the other claims.

8. CONCLUSION

In view of the preceding discussion, Appellants respectfully request that the rejection of claims 1, 3-7 and 9-19 be reversed and that these claims be allowed.

Respectfully submitted,

9/7/2006
Date

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Appendix A -- Claims Appendix

The claims on appeal are:

1. A preventive treatment method for a multilayer semiconductor structure that includes a support substrate, at least one intermediate layer of insulator material and a surface layer of semiconductor material in which the surface layer is to be subjected to a subsequent chemical treatment, which method comprises: forming a protective layer between the intermediate layer and the surface layer, with the protective layer being made from a material chosen to be sufficiently resistant to the chemical treatment to protect the intermediate layer from chemical attack during the subsequent chemical treatment of the surface layer of the multilayer semiconductor structure; forming a structure by bonding a donor substrate to the support substrate; and then transferring at least the surface layer from the donor substrate to the support substrate by a layer transfer technique to form the multilayer semiconductor structure.

3. The method of claim 1 which further comprises providing the intermediate and protective layers on a surface of at least one of the support substrate and the donor substrate before bonding.

4. The method of claim 1 which further comprises providing the intermediate layer on a bonding surface of one of the substrates and the protective layer is provided on a bonding surface of the other substrate before bonding.

5. The method of claim 1 wherein the surface layer is transferred by providing a weakened zone in the donor substrate at a depth sufficient to define the surface layer, bonding the surface layer of the donor substrate to the protective layer and then detaching the surface layer from the donor substrate.

6. The method of claim 5 wherein the weakened zone is provided by at least one of implanting atomic species in the donor substrate to a predetermined depth, or by providing a porous layer in the donor substrate.

7. The method of claim 1 which further comprises forming the multilayer semiconductor structure by bonding a donor substrate to the protective layer and then obtaining the surface layer by at least one of chemically etching, grinding, polishing, using CMP, or abrading the donor substrate.

9. The method of claim 1 wherein the intermediate layer at least partly forms an insulating layer of the structure.

10. The method of claim 9 wherein at least a part of the intermediate layer is made of SiO_2.

11. The method of claim 9 which further comprises forming the intermediate layer by oxidation.

12. The method of claim 1 wherein the protective layer forms at least a part of the insulating layer of the structure.

13. The method of claim 1 wherein the protective layer is made from a nitride material.

14. The method of claim 13 wherein the protective layer is made of Si_3N_4 or SiON.

15. The method of claim 1 wherein the layer transfer is facilitated by providing the donor substrate with a weakened zone beneath the layer that is to be transferred to the support substrate.

16. The method of claim 1 wherein the protective layer is formed by depositing a nitride on a bonding surface of the donor substrate or the support substrate.

17. The method of claim 1 which further comprises providing the multilayer structure with a weakened zone at the bonding interface by providing at least one of the two layers with a rough surface.

18. The method of claim 17 which further comprises utilizing a chemical treatment to roughen the surface of at least one of the two layers before bonding.

19. The method of claim 1 wherein the chemical treatment of the surface layer includes a chemical treatment based on hydrofluoric acid.

Appendix B -- Evidence Appendix

None

Appendix C -- Related Proceedings Appendix

None